Evaluation of Advanced Si and SiC Switching Components for Army Pulsed Power Applications

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Abstract — Super gate turn-off thyristors implemented in both silicon and silicon carbide semiconductors were investigated for high-voltage, high-current pulsed power applications. Modular 80 kA and 400 kA switches implemented in silicon (2.0 cm^2 dies) and individual silicon carbide switch die (0.16 cm^2) were evaluated. The Si 80 kA and 400 kA switches were demonstrated (at ambient temperature) to provide rates of current rise (10-90% peak current) and peak currents (145 μs width) of 24 kA/μs and 92 kA; and 40 kA/μs and 400 kA, respectively. The Si 80 kA switch was repetitively pulsed 1000 times with no significant performance degradation [5]. The SiC switch die were demonstrated to provide specific rate of current rise and current density of 49 kA/μs/cm^2 and 56.1 kA/cm^2, which are at least 2.5 times greater than are possible in silicon pulse switches [5], [6]. The SiC switches were repetitively pulsed at 5 Hz up to 99,000 times without failure and were demonstrated to operate at case temperatures up to 150°C.

I. INTRODUCTION

The U.S. Army Research Laboratory (ARL) is investigating the switching capabilities of advanced silicon (Si) and silicon carbide (SiC) devices for high current and high voltage pulsed power applications. These solid state switches are intended to replace more traditional vacuum and single-wafer thyristor switches in Army applications such as electromagnetic (EM) mortar and EM gun. The benefits of these advanced Si and SiC switches are higher di/dt, higher peak power levels, increased reliability and lifetime, higher current densities and smaller switch volume. ARL is collaborating with Silicon Power Corporation (SPCO) and Cree Inc. to evaluate the enhanced performance of super gate turn-off thyristors (SGTOs) implemented in Si and SiC, respectively, and improve packaging for pulsed power applications.

The cell-based SGTO approach provides for extremely high turn-on gains (with drastically reduced gate-drive requirements) and negates the need for a bulky clamping

apparatus required for the traditional single-wafer thyristor. By implementing modular switches using the SGTO cells, high rate of current rise and action (that previously had only been demonstrated by vacuum switches) can be attained in the most compact and reliable switch possible [3]. Si SGTOs are being investigated as a near-term solution for Army pulse power requirements and 4H-SiC SGTOs are being investigated as the far-term solution which should provide even higher action, rate of current rise and power density due to SiC's enhanced material properties over those of Si: bandgap (3.2 eV), thermal conductivity (3.0-3.8 W/cm*K) and critical field ($2.2x10^6$ V/cm) [1], [2].

II. EVALUATION OF 80 KA SILICON SGTO

A. Design

The basic Si SGTO module, shown in Fig. 1, was designed by SPCO [3]. It consists of eight SGTO switch die with a common anode and two parallel cathode terminals which maintain the module as two parallel, semi-isolated switches. Each SGTO die is rated for 10 kA forward conduction, 3.5 kV forward blocking and a suggested action of 17.3 kA^2s. Each module is therefore capable of 80 kA and 3.5 kV. Depending on the pulse width of the current, the modules may be used to achieve greater than 90 kA. Gate current enters the module at one point and is distributed via a PC board to the eight SGTOs in parallel. The Si modules are designed to be used in multiple parallel and series combinations and thus may be appropriate in a wide range of applications.

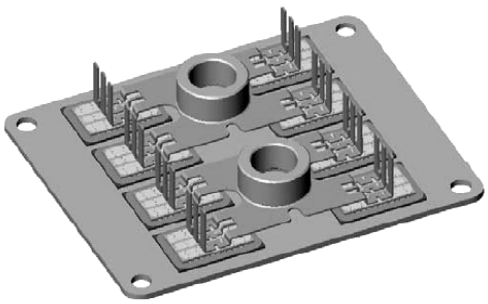

Fig. 1. Interior of one Si SGTO module.

The 80 kA, 7 kV SGTO is created by stacking two modules in series, as shown in Fig. 2. High voltage is evenly distributed across the two layers by a parallel resistor network of 960 kohm per module. A single gate driver board is utilized with an isolation transformer. The 80 kA SGTO seen in Fig. 3 can be operated at 10 kV by adding two more layers of modules for safe voltage distribution.

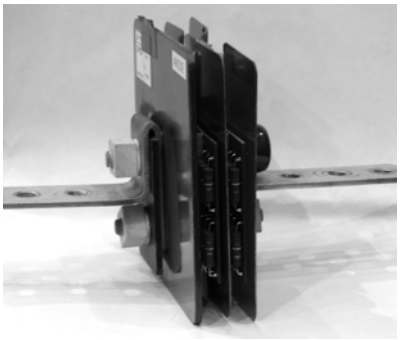

Fig. 2. 80 kA, 7 kV SGTO switch.

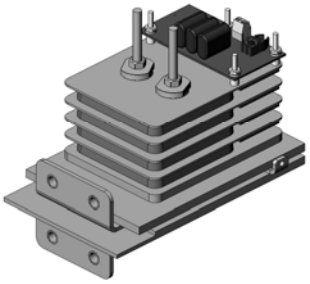

Fig. 3. 80 kA, 10 kV SGTO switch.

B. Experimental Procedure

The 80 kA, 7 kV switches were first high-potted to full voltage, then inserted into a basic RLC ring down circuit, as shown in Fig. 4, with a resistive load of 0.086 ohm. The devices were switched at 200 V intervals up to peak current. They were then

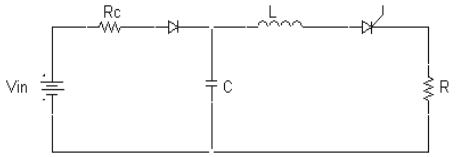

Fig. 4. Schematic of basic ring down RLC circuit.

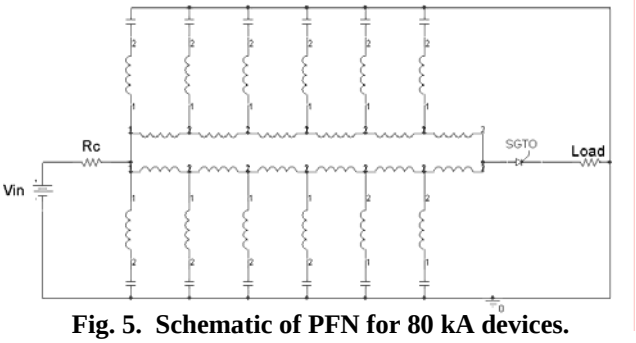

Fig. 5. Schematic of PFN for 80 kA devices.

transitioned to a dual pulse forming network, shown in Fig. 5, designed at ARL to produce 80 kA, 145 µs current pulses at 6.5 kV. After single shot testing up to peak current, capacitors were removed from the charging end of the PFN to shorten the width to about 120 µs in preparation for switch lifetime and reliability testing. The PFN was isolated from the power supply during the SGTO's switching event by a mechanical switch which was automatically triggered by a signal from a pulse generator. When the PFN had completed charging, it was disconnected from the power supply and the SGTO was triggered. The high voltage power supply was reconnected seconds later to give the SGTO ample recovery time. A large fan was aimed toward both the switch and the carbon washer style resistors used for the load, because the nearest resistors tended to heat up after multiple current pulses. The carbon washers from Carborundum have a peak energy rating of 79.5 kJ and a maximum temperature of 230º C. The goal of this testing was to evaluate the lifetime of the switch up to 1000 shots at 80 kA.

The 80 kA, 10 kV switches were similarly high-potted and tested to rated current in an RLC ring down. Current balance between the two halves of each switch was monitored at the two cathode terminals. For applications requiring greater current levels, two of these 80 kA, 10 kV SGTOs were connected in parallel. A dual transmitter was connected to two equal fiber optic cables which were used to trigger the separate gate drivers. Timing was monitored according to when a MOSFET on the gate driver board switched and began to drop the voltage on the driver's 24 V storage capacitors. One pair of 80 kA devices was tested in the ring down circuit in two different physical configurations to determine if there would be any effect on current balance. The switches were first set up facing each other, then positioned side by side. The pair of devices was next used to switch a capacitor bank into an inductive load of about 0.024 ohm, as diagramed in Fig. 6. A high voltage diode clamp was connected in anti-parallel with the switches to protect them from any negative current. The focus of the test was to verify that two separately driven switches could be triggered simultaneously and evenly share forward flowing anode-to-cathode current.

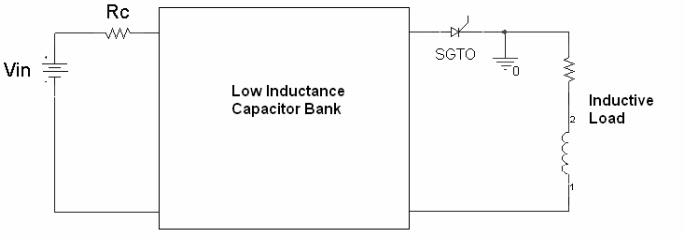

Fig. 6. Schematic of inductive circuit used for paired 80 kA switches.

C. Results and Discussion for 80 kA Switch Evaluation

In the ring down circuit, each 7 kV unit was brought up to 73 kA and 24 kA/µs (Fig. 7) before being moved to the PFN. Performance of the two different switches was nearly identical. At 6.6 kV in the dual PFN, the current through the same SGTOs peaked at 92 kA with a rise time of 15 kA/µs and a pulse width of 145 µs (Fig. 8).

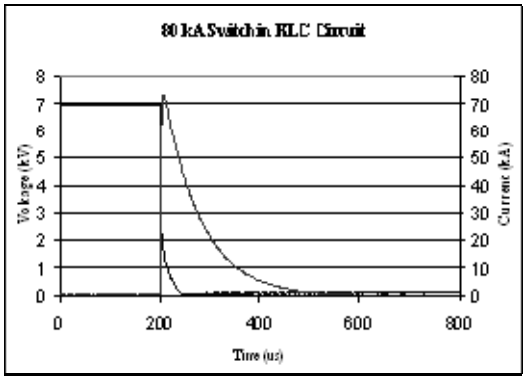

Fig. 7. 80 kA ring down voltage and current waveforms.

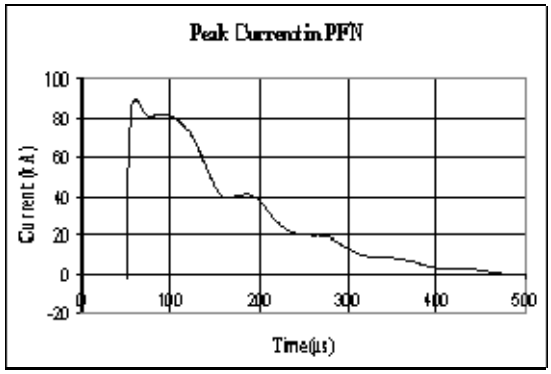

Fig. 8. 80 kA PFN current waveform.

For the lifetime testing, one thousand single shots were completed without failure and without any notable change in pulse shape. Although two 7 kV units were successfully tested in both the ring down and the PFN, only one switch survived 1000-shot testing because of an unrelated error which shorted out the load while the other 7 kV switch was under testing. Further lifetime evaluation is planned, as well as repetitive rate switching of the modules. Before that can take place, a high power charging circuit needs to be designed and implemented.

When the 80 kA, 10 kV devices were evaluated, much of the focus was on how well the two halves of the modules shared current. The sharing of six individual switches was monitored in the ring down circuit. Sharing varied from 50%/50% of total anode-cathode current through the two cathode rings of one switch to 51%/49% distribution in the 80 kA units. When two of these switches were triggered from a dual transmitter, repeated testing showed that the gate drivers triggered one nano-second apart, as shown in Fig. 9. Peak current distribution at the four cathode rings was 26%, 25%, 24% and 25% when the switches faced each other, and 25% all around when the switches were side by side (Fig. 10). It was decided that either configuration was acceptable.

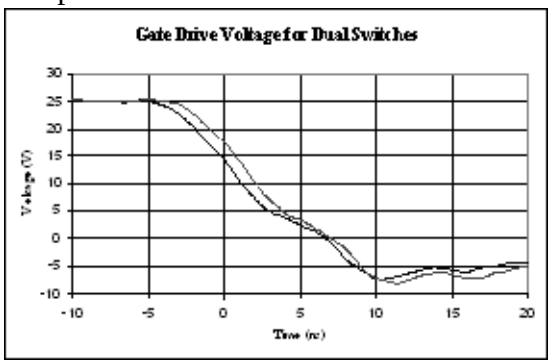

Fig. 9. MOSFET trigger timing for two 80 kA switches.

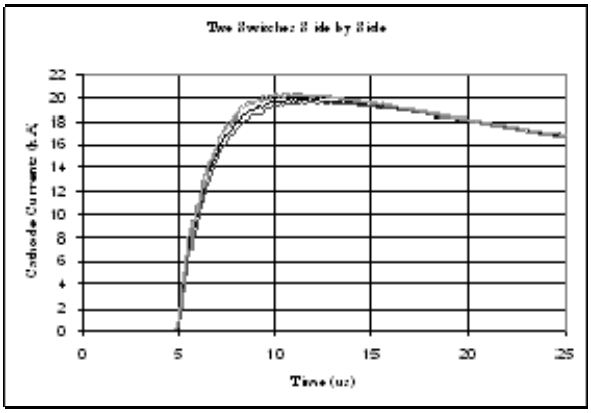

Fig. 10. Cathode currents for two 80 kA switches.

III. Evaluation of 400 kA Silicon SGTO

A. Original Design

The 400 kA, 10 kV SGTO is created by joining six modules in parallel, three layers deep. A resistor network of 430 kohm per layer is used to distribute 1/3 of the high voltage to each layer of modules. The gate driver is similar to that of the 80 kA switch but scaled up to provide enough gate current for 18 modules. This SGTO design can be seen in Fig. 11.

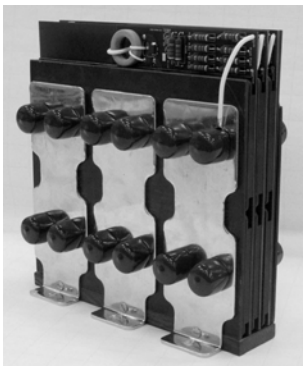

Fig. 11. Original 400 kA switch.

B. Experimental Procedure

The initial delivery of 400 kA switches was tested in a ring down circuit with minimum inductance to evaluate peak current rise and to maintain focus on the forward current pulse by limiting any negative swing. For the first rounds of testing, the SGTO units were switched at 200 V intervals so that if any problems were met, the particular voltage or current level causing the trouble could be narrowed down more easily. Because the voltage dropped across the load was much lower than the applied voltage, more resistor stacks had to be added in parallel to reach the high current levels desired. One switch carried 176 kA at 26 kA/μs during a test shot at 8.4 kV. When 9.1 kV was applied to the anode, the switch self-triggered. High voltage was again applied to the anode and measurements taken across each layer of the switch showed that all of the voltage was now being dropped across one layer, and the other two layers appeared shorted. A second switch reached a current level of 216 kA and 35 kA/μs before it was noted that one layer of the device was shorted. When high voltage was again applied to the anode of this switch, the voltage was being shared across two layers whereas the voltage drop on the third layer read zero. It was later determined that a corner module on that layer was shorted internally anode to cathode. Similarly, the other switch also had an internally shorted module on each faulty layer.

Because of a concern that the soft gel epoxy used in the modules might allow particles to creep through the material during current flow and cause damage, SPCO replaced the failed modules with new ones that were potted with a hard epoxy. Voltage balancing wires were added externally where the front layer of modules connected to the anode buss. The voltage drop across each layer of modules was consistently monitored, though at higher voltage and current levels, the high voltage probes seemed to pick up a lot of noise from electric-magnetic fields. After successfully reaching 298 kA and 38 kA/μs at 9.7 kV applied, the ring down circuit was reconfigured with larger capacitance and a smaller resistive load to reach full desired current with minimal, if any, undershoot. Both switches were individually tested up to 180 kA at 5 kV, at which point it was found that the rear layer of each switch was again shorted. It was also found that some of the gate current “steering diodes” at the secondary of the driving transformer had shorted. These were replaced with more robust diodes and a “new” 400 kA switch was constructed out of three remaining functional module layers. Successive test shots were conducted, creeping up to the previous point of failure and measuring more points on the switch along the way. At 4 kV, the voltage measured across the anti-parallel gate-cathode diode was as high as 55 V and had increased every time the anode

was raised. The diode originally in position there could only handle 60 V in the reverse bias. Also, besides monitoring total current through the switch, Rogowski coils were places around the three "legs" and it was found that the stack of modules nearest the load carried about half of the overall current, whereas the two farther legs only carried about 1/4 each. This discovery inspired further current sharing measurements which revealed that the upper row of modules carried much less current than the lower row. The lower corner modules near the load, which had failed more than once, were found to carry the highest portion of the current, suggesting that the repeated high current failures of modules in that location were probably the result of over-stressing that module with current and heat.

After this discovery, the 400 kA boards were tested one layer at a time in various physical layouts. Current imbalances were easily shifted from one module to another by orienting the boards in different physical layouts. Steel bolts which were isolated from both high voltage and ground were used to compress the anode and cathode connections of the modules. A voltage probe placed on these bolts during test fire showed small voltage spikes, suggestive of high electromagnetic fields within the area of the switch. Trial and error showed that these fields could be minimized and current balance between modules could be improved by redesigning the layout.

C. Results and Discussion for 400 kA Switch Evaluation

ARL and SPCO worked together to modify the 400 kA unit and are preparing to apply for a patent for its redesign. Details will not be published until patent disclosure. The new 400 kA switches were pulsed with both resistive and inductive loads. With a resistive load of 0.015 ohm and an 860 µF capacitor, the SGTO switched 376 kA with a rise time of 40 kA/µs (Fig. 12). The load was then moved to a larger energy storage bank to achieve the full 400 kA at 8.8 kV, as shown in Fig. 13. The two cathodes rings of each module were monitored for current output, and the sharing between cathodes only varied by 11% over and 7.5% under the ideal shared current, which for the data shown in Fig. 14 would have been 8.7 kA per cathode. One switch has so far been successfully pulsed nine times at 350 kA with an action of 8.8 MA^2s.

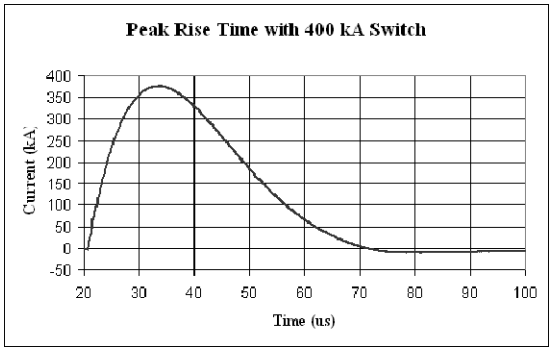

Fig. 12. 400 kA ring down current waveform.

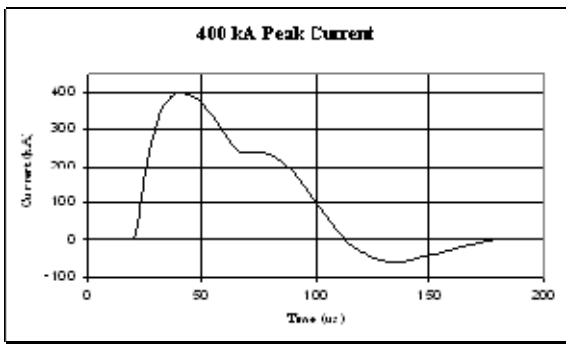

Fig. 13. Peak current with 400 kA switch.

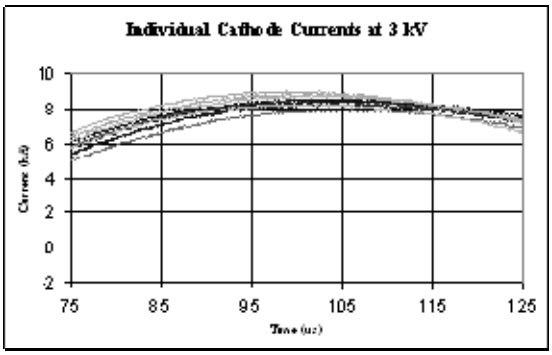

Fig. 14. Current balance for twelve cathodes of 400 kA switch.

IV. Evaluation of Silicon carbide SGTO

A. SiC Device Design

The SGTOs tested in this study have a 4H-SiC layered structure with an overall area of 4 mm by 4 mm. The active area of the mesa is 0.07 cm^2. Some of the devices tested are designed with interdigitated anode / gate fingers whereas others have the anode and gate laid out in concentric circles. All thyristors were turned on with a negative current applied to the gate relative to the anode.

Devices were characterized on a programmable curve tracer prior to circuit testing. They had a typical anode-gate forward voltage drop of 2.6-2.8 V and a reverse anode-gate voltage holdoff of at least 17 V. The best devices started with anode-to-cathode current leakage of less than 5 µA at a blocking voltage of 1000 V. Devices that showed small leakage at lower voltage levels were also used.

The devices characterized were obtained from three CREE Inc. wafers and packaged at ARL (as shown in Fig. 15). The pitches, or distances between repeating gate patterns, varied among 25 µm, 28 µm, and 40 µm. The wafer number and pitch did not seem to affect the test results obtained for each thyristor, though those probe-tested within the wafers above 1100 V at CREE were able to reach higher voltage and current levels in the circuit. The interior package space around the bond wires and the die was initially filled with a silicon-based potting compound to ensure voltage isolation. This potting compound appeared to cause problems when the packaging was raised to temperatures exceeding 125° C. It is believed that expansion and contraction of the compound was pulling on the gate and anode wires. For this reason, most of the devices tested at temperature did not contain any isolating compound. The anode to cathode voltage was kept to about 700 V to prevent flashover.

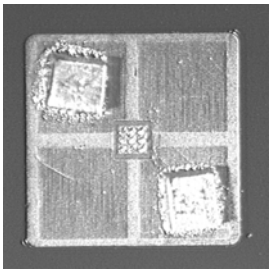

Fig. 15. SiC device.

B. Experimental Procedure

The evaluation circuit was designed to reach a peak current of 4 kA at about 700 V. Four paralleled capacitors provided 20 µF of storage. A 1 kV, 20 mA power supply was used to charge the capacitors through a protective diode and a charging resistor of 6.25 kohm. For each shot, a 5 µs signal was sent to the driver board which then applied a maximum anode-to-gate current of 1.2 A. The anode and gate connections were tied by 5 ohm of resistance. The capacitors discharged through the switch into a load of 0.11 ohm. The goal for the first stage of testing was to determine the peak attainable current for these devices. The next goal was to see how many high current pulses the thyristors could survive at repetitive rates. Finally, the packaging was raised above ambient temperature to examine what effects heat would have on peak attainable current and repetitive rate results. Evaluation of SiC performance at wider pulse widths and higher di/dt will take place in the near future.

To establish the peak current for these devices, ten thyristors were tested by increasing V_{AK} in 50 V increments until failure. Current and rise-time values were relatively constant at a given voltage during testing of each device, but the maximum voltage or current that each individual switch could survive varied. The devices were removed from the circuit and characterized on a curve tracer at regular intervals to monitor degradation. Failure was defined as the point at which the thyristor would begin

to self-trigger or when the anode-cathode leakage current began to limit voltage held by the capacitors. Failed switches were examined for exterior signs of damage, and those with obvious burn marks were photographed using 5x and 10x lenses and a scanning electron microscope.

Testing at a repetitive rate was conducted up to 5 Hz at various currents in the same circuit configuration. Nineteen thyristors were evaluated during this stage of analysis. The charging resistance was decreased to 530 ohm to decrease the RC time constant, and a higher current power supply was used for more rapid charging. If a thyristor failed short or began to leak 150 mA of current, the power supply would trip and automatically turn off. Switching waveforms were captured using an oscilloscope, and at the end of each stage of testing, data from all thyristors were compared and analyzed.

The effects of temperature were monitored both on the curve tracer and during pulsing. The thyristor packaging was sequentially raised to 75°, 100°, 125° and 150° C by varying the current through a high wattage resistor which was attached to the cathode base plate of each thyristor evaluated. In the same ring down circuit used for earlier testing, a resistor current of 1.3 A was used to maintain the temperature at 150° C ± 2° measured. Temperature was monitored using a K-type thermocouple and compatible meter.

C. Results and Discussion

The device parameters measured during each test shot included the differential voltage from anode to cathode, the voltage drop across the load resistor and the gate current. The maximum anode voltage applied in the final circuit design was 660 V. The maximum voltage measured across the load during that test was 430 V. This value was divided by the load resistance (0.11 ohm) to calculate a peak current of 3.9 kA. A graph of this maximum current data may be seen in Fig. 16. Overwhelming anode-cathode leakage current would not allow the applied voltage to be raised any higher, and the 660 V shot was repeated once before the switch began to self-trigger. Changes in leakage current can be seen in Fig. 17. The maximum 10%-90% rise-time of current was 7.8 kA/μs or 49 kA/μs/cm^2. The action of the current pulse was 25 A^{2}s. When the failed devices were photographed under the microscopes, burn marks and melting of the silicon carbide were seen at failure points (Fig. 18 and 19). Post-failure voltage application

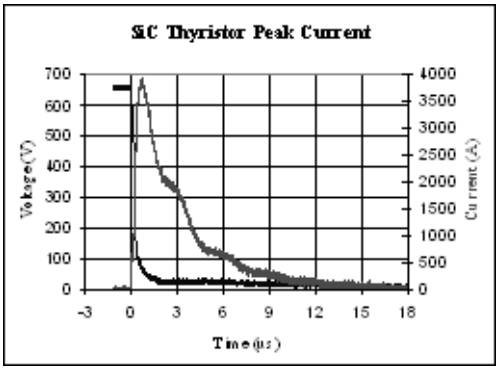

Fig. 16. Voltage and current waveforms for SiC switch.

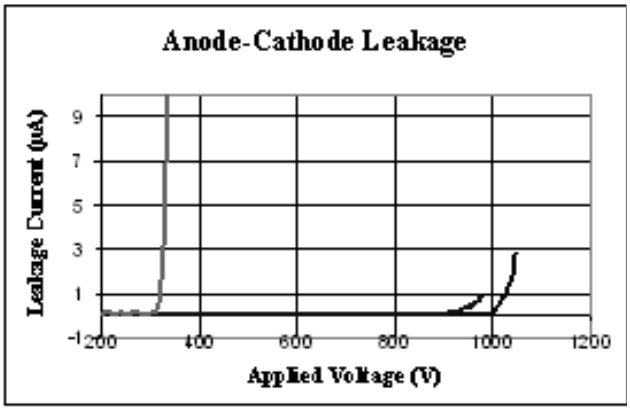

Fig. 17. Increase in anode-cathode leakage as a function of pulsed current. Before testing, this device did not begin to leak until at least 1000 V were applied. After single-shot testing up to 1.6 kA, the device began leaking at 900 V. After continuing up to 2.8 kA, the current leakage climbed sharply starting at just over 300 V.

on the curve tracer showed that although not all devices became shorted A→G, all had severe current leakage in the layers between the gate and cathode.

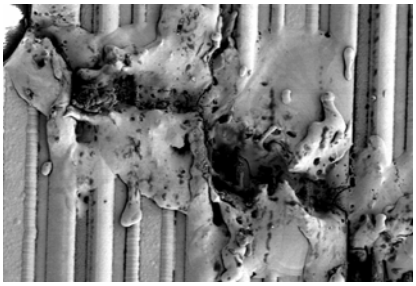

Fig. 18 and 19. Burn track through gate and anode fingers terminating at edge of device. As seen with 10x zoom lens and SEM.

The SiC thyristors were pulsed at repetitive rates of 1 Hz and 5 Hz at ambient temperature. It was found that at a peak current of 2 kA, a device could survive as many as 99,000 pulses at 5 Hz. Once current was increased to 2.5 kA or 3 kA, though, anode-to-cathode voltage holdoff usually began to drop by the time one dozen shots were completed. Other specific SiC thyristors lasted 25,101 pulses, 6747 pulses and 3500 pulses at 2 kA and 5 Hz.

A third group of SiC SGTOs was evaluated at single shot and 5 Hz rates up to 150° C. The highest single shot current attained at 150° C was 3.2 kA with a pulse width of 2 μs. Other devices were switched at 2.5 kA without failure for each temperature: 75°, 100°, 125° and 150° C. It was noted that rise times were greater at temperatures above 75° C even at lower current levels. A peak 10%-90% rise time of 9.0 kA/μs was obtained at 75° C. The higher rise time at temperature may be a result of switch behavior or characteristic changes of other circuit components, such as the load resistors and the copper sheet metal used for bussing. Further study of rise time needs to be completed.

Switching at about 2.6 kA, 5 Hz and 150° C was conducted on three devices for thousands of shots. The longest surviving device lasted 14,655 pulses at this level, whereas another ran for 13,930, plus extensive 5 Hz testing at lower currents. As with the room temperature testing, the most limiting factor for the SiC thyristors seems to be pulsing at currents of 3 kA or more. Devices tested at temperature have not yet been analyzed with the scanning electron microscope, but no external burn tracks are visible under a 10x microscope lens.

Most of the devices tested at room temperature had silicon-based potting for voltage isolation, but the potting appeared to be a problem early on in high temperature testing. In retrospect, further repetitive rate testing should be conducted with un-potted devices in case the extra heat insulation was limiting performance. One potted device was used for 100° C repetitive rate work at 2 kA and 5 Hz. Unlike the devices pulsed with potting at ambient temperatures, it only survived 265 switching events before shorting anode to cathode.

V. SUMMARY

It has been shown that silicon and silicon carbide SGTOs can be used in high power pulsed applications. The 80 kA units tested achieved currents as high as 92 kA and pulse widths as wide as 145 μs. They also survived 1000 single shots and reached a peak di/dt of 24 kA/μs. The 400 kA SGTOs have also been switched multiple times at full current with a pulse with of 90 μs. Silicon carbide SGTOs survived repetitive rates up to 5 Hz and temperatures up to 150° C. The next stages of device evaluation will

include determining recovery time of the 80 kA Si modules, testing how much negative current the modules can handle, and rapid repetitive switching of both the 80 kA and 400 kA units. The SiC devices will go through further failure analysis, and the pulse width and rise time will be varied to establish the SGTO's limits.

Acknowledgements

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References

[1] S.B. Bayne and D. Ibitayo, "Evaluation of SiC GTOs for pulse power switching," *14th IEEE International Pulsed Power Conference Proceedings*, June 15-18, 2003, pp. 135-138.

[2] "Silicon carbide substrates: product specifications," Cree, Inc., Durham, NC, Version MAT-CATALOG.00D, Revised Jan. 2005.

[3] V. Temple, " 'Super' GTO's push the limits of thyristor physics," *35th Annual IEEE Power Electronics Specialists Conference Proceedings*, June 20-25 2004.

[4] B. Jayant Baliga, Power Semiconductor Devices. Boston: PWS Publishing Co., 1996.

[5] R.L. Thomas, H. O'Brien, W. Shaheen, S.B. Bayne, "Evaluation of a 7 kV, 80 kA SGTO module," 15th IEEE International Pulsed Power Conference, June 13-17, 2005.

[6] H. O'Brien, W. Shaheen, S.B. Bayne, "Pulsed power Ssitching of a 4 mm x 4 mm SiC thyristor," 15th IEEE International Pulsed Power Conference, June 13-17, 2005.

[7] T. F. Podlesak, R. L. Thomas, F. M. Simon, "Preliminary evaluation of super GTOs in pulse application," *IEEE Transactions on Plasma Science*, Vol 33-4 pp. 1235-1239, August 2005.